



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



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High Performance D2D PHY IP and Other Soft IP Relevant to AI

Letizia Giuliano

DAC Engineering Track Session: The Open Chiplet Economy and AI

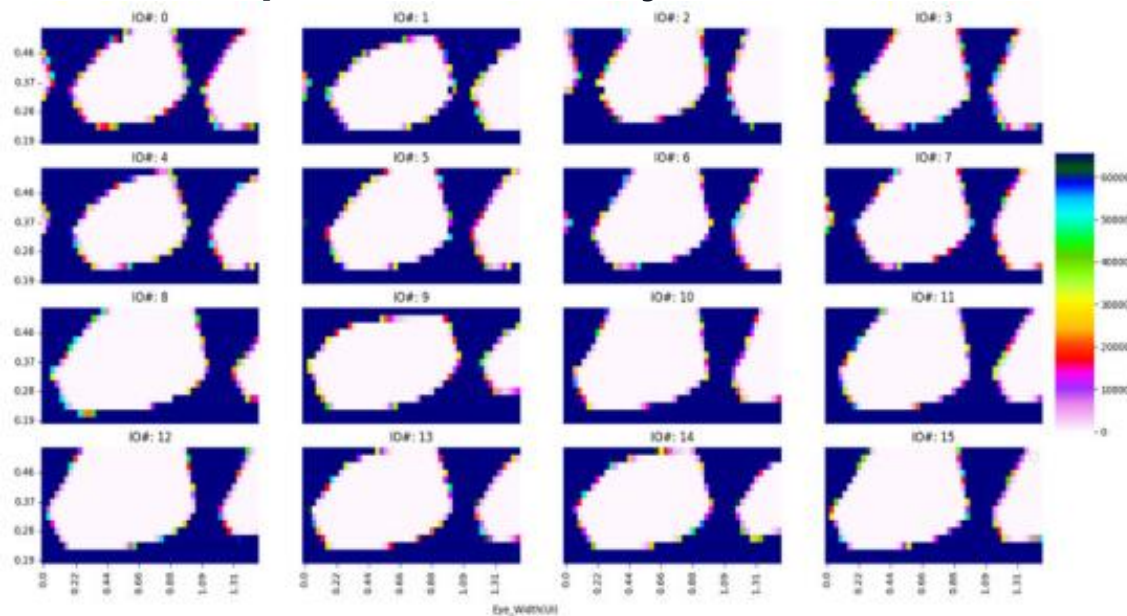
Tuesday, June 25, 2024



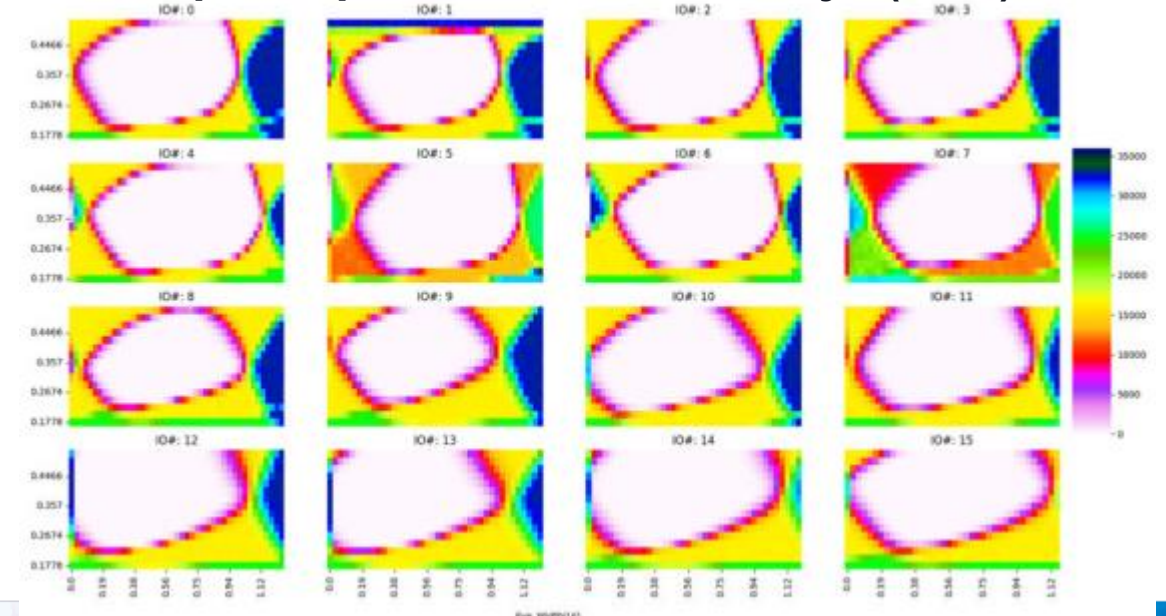
UCIe N3 24G Silicon Results – Executive Summary

- Early standard package measurement results align well with system simulation
- Working to build BER metrics for eye height/width
- Regression tests in place to evaluate calibrations over large number of parts
- Team working to build all necessary calibrations for die-to-die

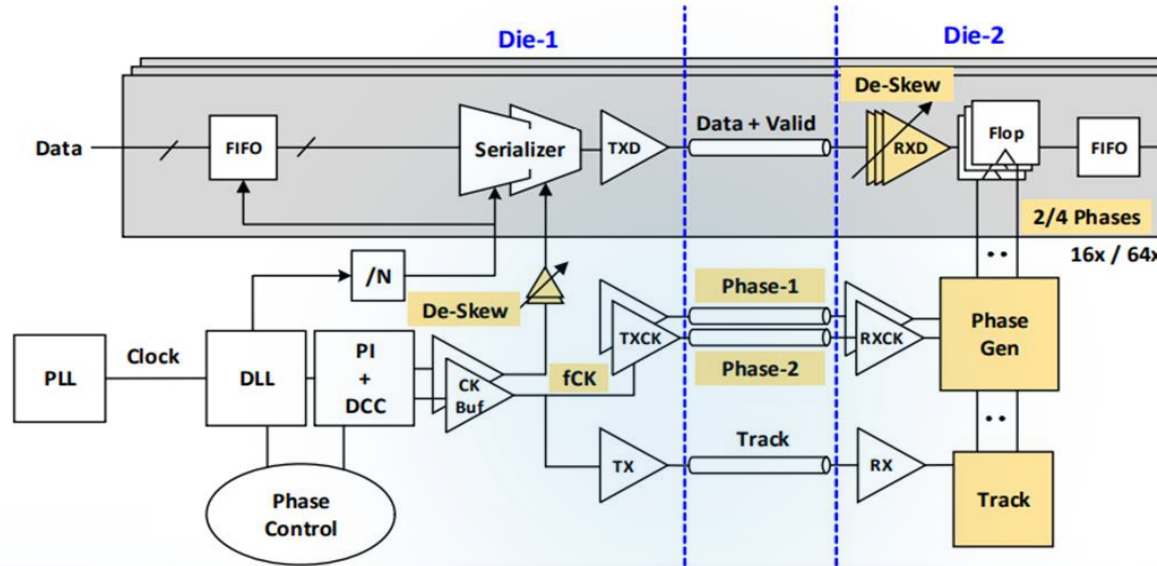
TX output destructive eye monitor at 24G



RX sampler input non-destructive eye (NDE) at 24G



D2D UCle Architecture Optimizations



Parallel Interface

- Single Ended, Forwarded clocking
- Simple Tx and Rx help achieve Higher Density for Advanced package
- Optional Equalizations
- **Very Low Power 0.25-0.5pJ/bit**

Clocking

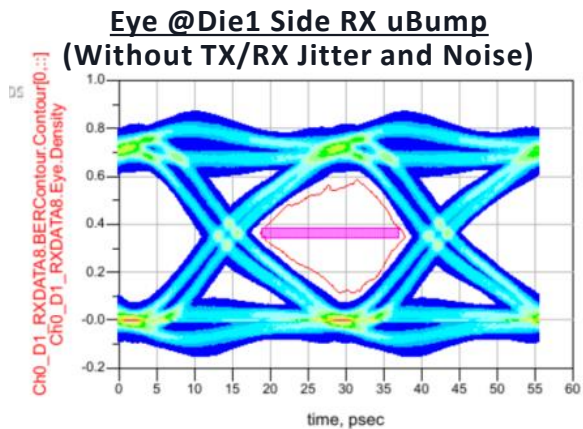
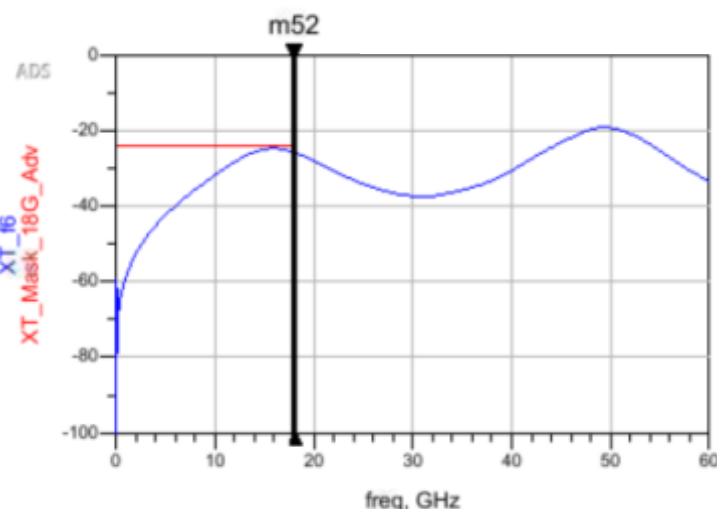
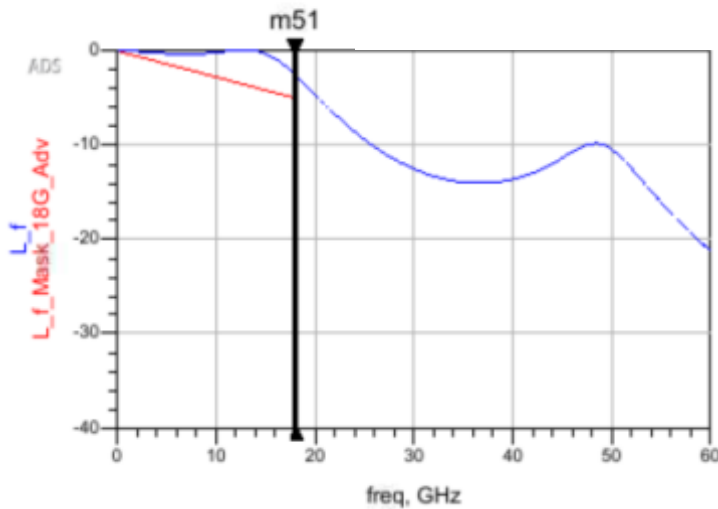
- Two differential-ended clock signals (Phase-1 & Phase-2)
- Rx generates clocks from the two clock signals to sample data signals
- Supports half-rate and quarter-rate clocks
- **Scalable architecture for Higher Data Rates**

TX and RX

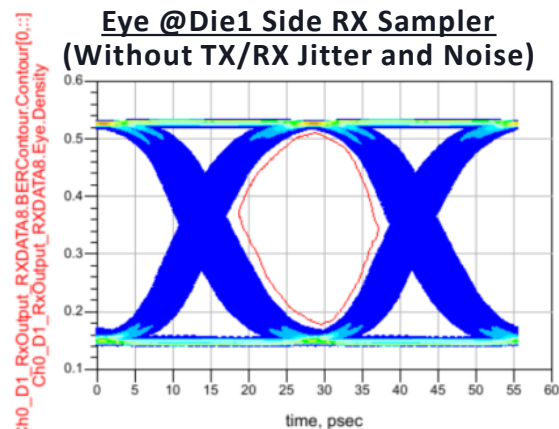
- Transmitter must be optimized topology for low power and wide VDDIO range
- Optional 1-tap FIR equalizations
- Receiver-matched architecture to minimize impact on supply jitter
- Track signal for reliable operations over VT
- **Reliable operation**

Package Routing Study for 32+Gb/s Advanced Package

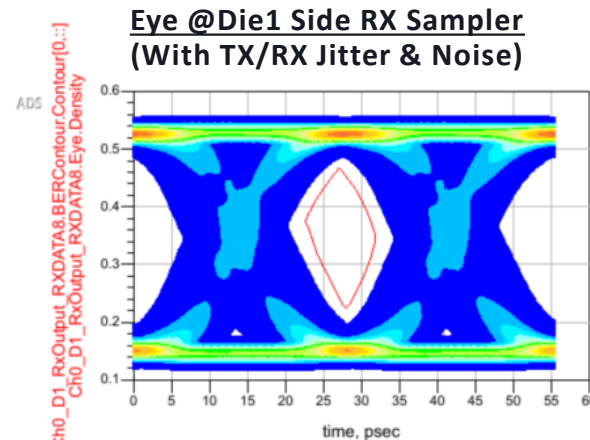
- Advanced package (CoWoS-R) channel analysis shows escape routing can meet UCle IL and Xtalk requirements up to 32+Gb/s
- Link performance meets requirements
 - Further optimization in progress on circuit design and EQ capability
 - Little EQ required



Measurement	...R.Height[0::]	Measurement	...ER.Width[0::]
HeightAtBER	463.0 m	WidthAtBER	19.2 p



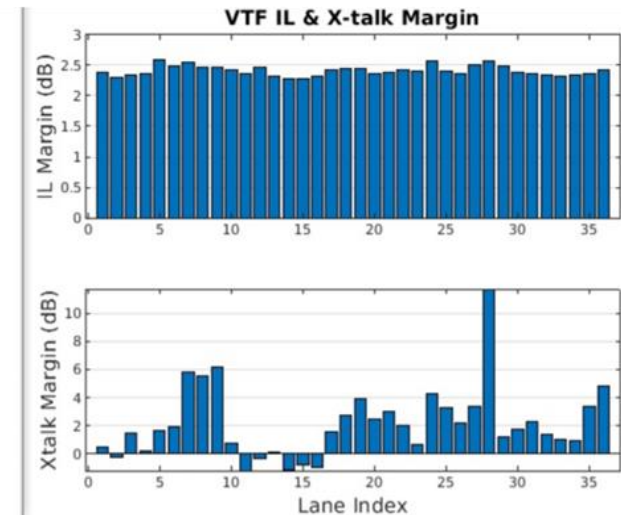
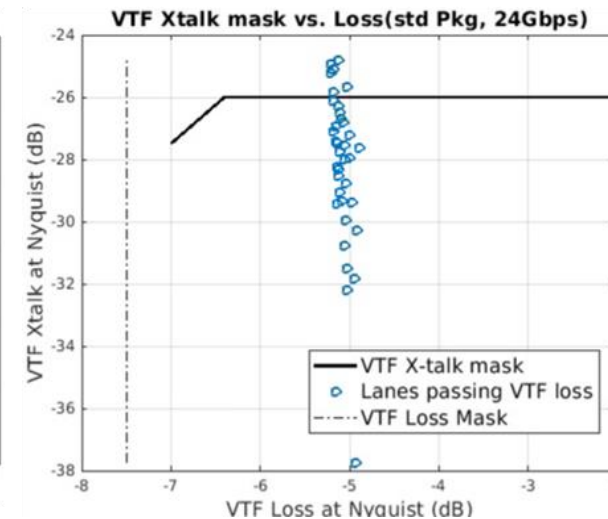
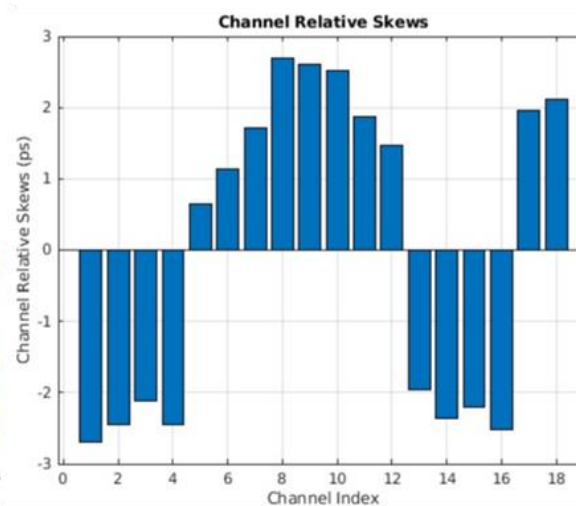
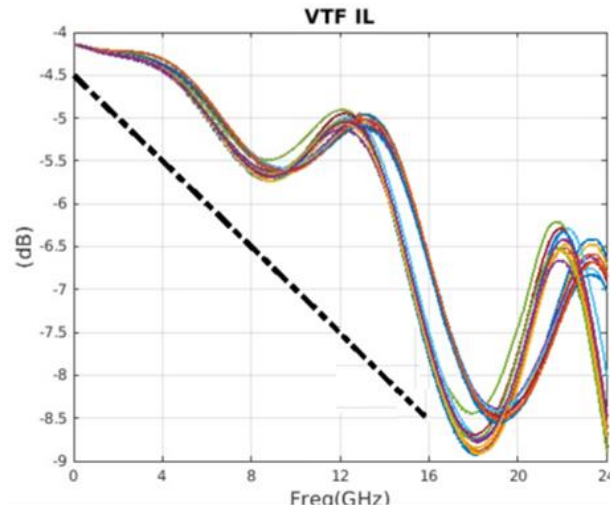
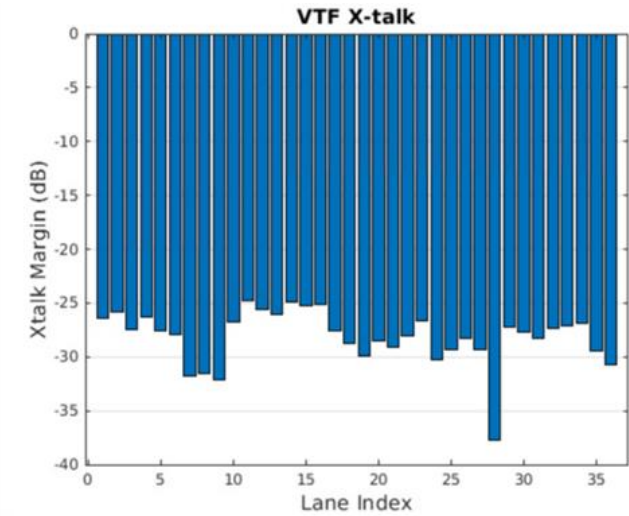
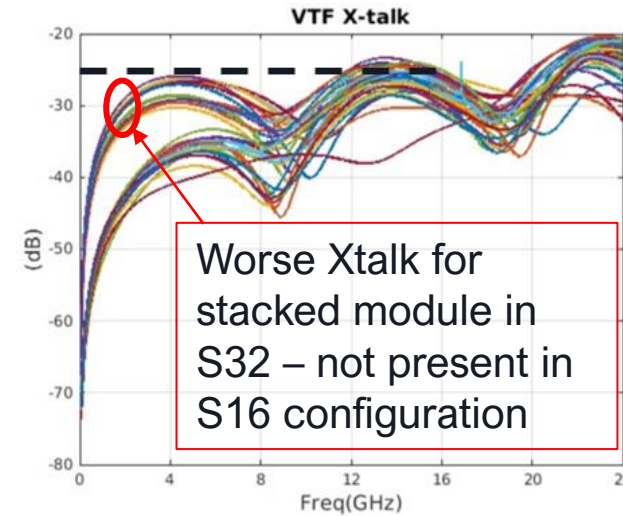
Measurement	...R.Height[0::]	Measurement	...ER.Width[0::]
HeightAtBER	330.0 m	WidthAtBER	18.6 p



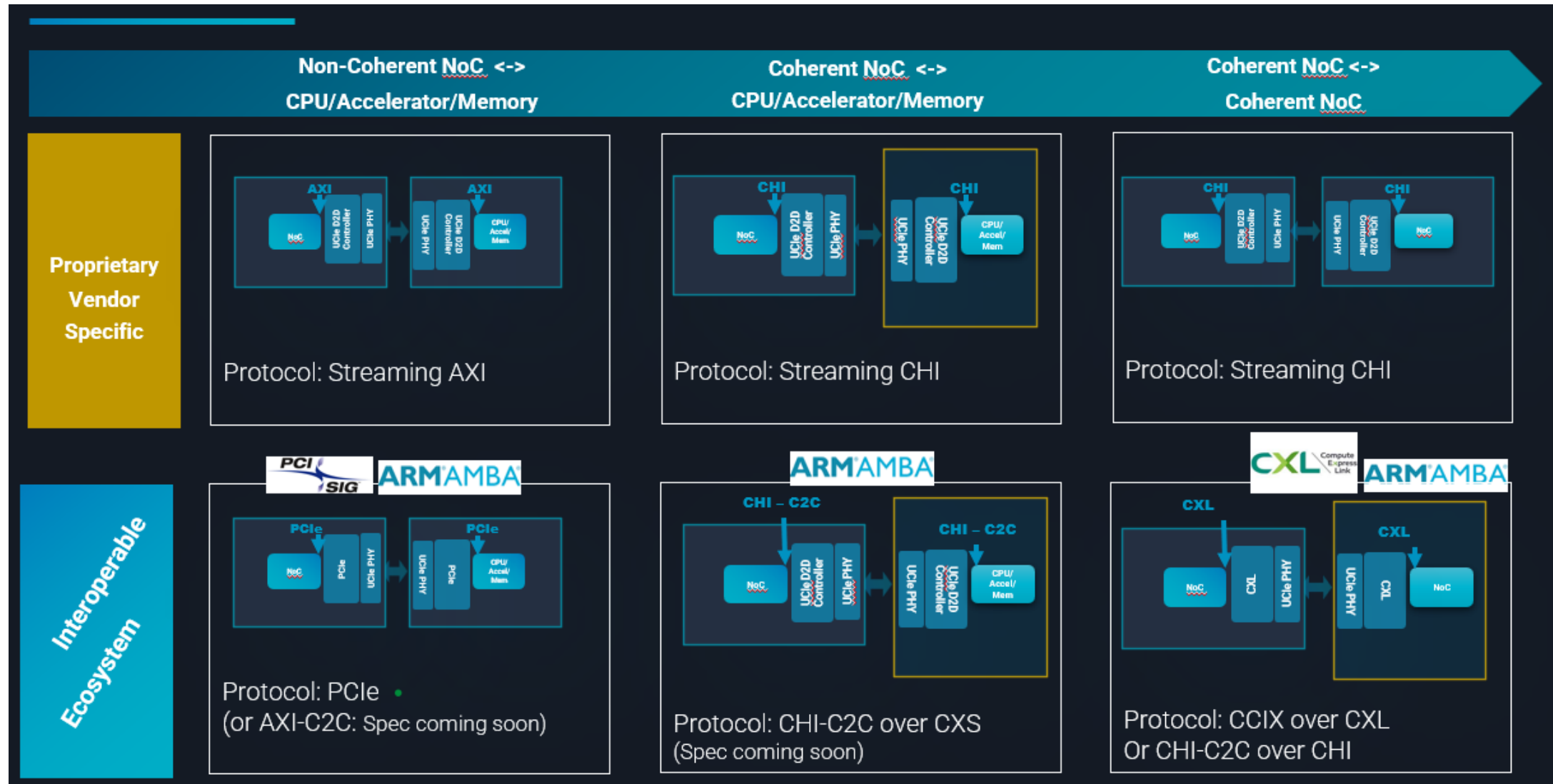
Measurement	...R.Height[0::]	Measurement	...ER.Width[0::]
HeightAtBER	231.0 m	WidthAtBER	9.31 p

Package Routing Study for 24Gb/s and 32Gb/s Standard Package

- Standard package channels:
 - Meet UCle IL requirements up to 32Gb/s
 - Meet skew requirements at 32Gb/s
- Link margin meets performance requirements with all impairments added
 - EH = 172mV; EW = 0.35UI in worst case channels



D2D Protocol Support and Use Cases



Alphawave SEMI UCle Offering

Alphawave SEMI UCle IP Solution



UCle 24G Generation 1

TN7/6 TN5/4 TN3 TN2 SF5 SF4X SF2

UCle- SP/ AP 16/24Gbps
AresCORE





UCle 32G Generation 2

TN7/6 TN5/4 TN3 TN2 SF5 SF4X SF2

UCle- SP/ AP 32+Gbps
AresCORE



Contact Alphawave for UCle Controller and PHY development plans

 Planned
 Available

Alphawave Semi High-Performance Connectivity Silicon IP

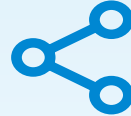
PCIe / CXL



High-speed Interface IP for data centre compute – CPU, GPU, AI & FPGA

PCIe 7.0 / CXL 3.1

Ethernet



112Gbps & 224Gbps PAM4 Interface IP for Networks – Switches, Routers, DPUs, NICs

400G, 800G, 1.6T Ethernet

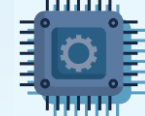
Memory IP



Memory Interface IP for SRAMs & HBM – CPU, GPU, AI, FPGA, DPUs

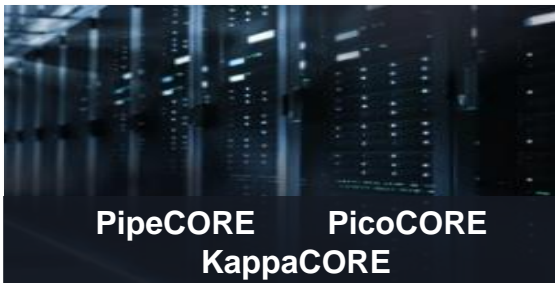
HBM3 and HBM4

Chiplets



Chiplet Interface IP 2.5D and 3DIC

UCle, Streaming, PCIe, CXL



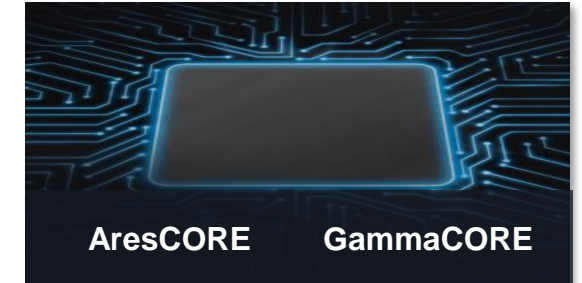
PipeCORE PicoCORE
KappaCORE



AthenaCORE ZeusCORE
OmegaCORE



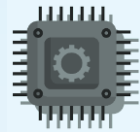
MidasCORE HermesCORE



AresCORE GammaCORE

Alphawave Semi Chiplets Portfolio

HIGH SPEED IO CHIPLET



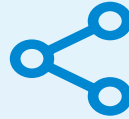
Multi-Standard SerDes IO with
Integrated Protocol Controllers and
UCle D2D

PCIe Gen6 / CXL 3.0 / 112Gbps
Ethernet



Multi-Standard SerDes / UCle

MEMORY IO CHIPLET



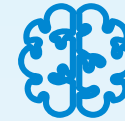
Low Latency, High Speed DDR5
and Memory Controller

DDR5 Memory Expansion



DDR5/UCle

ARM COMPUTE CHIPLET



High Performance, Arm-Based
Compute

Enables data acceleration

Arm Processor



Arm / UCle

Chipllets Enabled by UCle and Use Cases





Thank You!